PATENT

SYSTEMS AND METHODS FOR PRECURSOR CANCELLATION OF INTERSYMBOL INTERFERENCE IN A RECEIVER

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present invention is related to those disclosed in the following United States Patent Applications:

1. Serial No. [Docket No. 701075], filed concurrently herewith, entitled "SYSTEMS AND METHODS FOR OPTIMAL SYMBOL SPACING TO MINIMIZE INTERSYMBOL INTERFERENCE IN A RECEIVER";

2. Serial No. [Docket No. 701076], filed concurrently herewith, entitled "DUAL EQUALIZER FOR USE IN A RECEIVER AND METHOD OF OPERATION"; and

3. Serial No. [Docket No. 701259], filed concurrently herewith, entitled "SYSTEMS AND METHODS FOR OPTIMAL DISTRIBUTION OF SYMBOLS IN A FIXED SIZE DATA PACKET TO IMPROVE RECEIVER PERFORMANCE".

The above applications are commonly assigned to the assignee of the present invention. The disclosures of these related patent applications are hereby incorporated by reference for all purposes as if fully set forth herein.

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to wireless and wireline receivers and, more specifically, to a system and method for cancelling precursor intersymbol interference (ISI) in a receiver.

BACKGROUND OF THE INVENTION

The rapid advance of digital technology has created a great demand for, and corresponding advances in, wireless and wireline technology for communicating voice and data traffic. Much of this traffic is carried by the public switched telephone network over fiber optic cable and copper wire. Computers and other data equipment communicate over the Internet and a variety of proprietary local area networks (LANs) and wide area networks (WANs). Increasingly, various types of digital subscriber line (DSL) service or cable modem service are bringing broadband data into homes and offices. Many third generation cellular telephones and wireless PDA devices are also equipped to handle broadband data traffic and Internet capable.

However, even the most modern of wireless and wireline data

communication equipment still must contend with the age-old problems inherent in transmitting data through a channel from a transmitter to a receiver. Data is often transmitted as a series of pulses (or symbols) through a wire or the atmosphere. The data symbols may become distorted due to intersymbol interference (ISI), which is an overlap of adjacently transmitted symbols. In a wireless network, ISI may be caused by reflections of the transmitted symbols off natural objects (e.g., tress, hills) and man-made objects (e.g., buildings, brides) in the environment. The reflections cause multiple time-delayed, partially overlapping copies (echoes) of the same signal to arrive at the receiver. ISI also may occur in a non-linear, bandwidth limited channel if the symbol transmission rate is comparable to or exceeds the channel bandwidth, W.

Receivers frequently use a well-known technique, adaptive decision-feedback equalization, to minimize the effects of ISI. An adaptive decision-feedback equalizer (DFE) consists of a feedforward (or forward) filter, a feedback filter, and a decision circuit that decides or detects the value of each symbol in the received signal. The input to the forward filter is the received distorted sequence of data symbols. The input to the feedback filter is the sequence of previously decided (detected) symbols at

the output of the decision circuit. The feedback filter removes from the symbol presently being estimated that portion of the ISI that is caused by previously detected symbols.

There are limitations, however, to the performance of decision feedback equalizers. Even under the best of circumstances, a DFE occasionally makes an incorrect decision regarding the value of a received data symbol. The incorrect estimate is then propagated back to the feedback filter, thereby affecting decisions regarding subsequent symbols. Furthermore, a DFE almost always does not perform detection on the first copy of a symbol as it is received. Because of the performance of the channel, symbol reflections may combine in such a way that the peak power of the transmitted symbol occurs after the first echo of the symbol enters the DFE. Thus, some reflections of a symbol (postcursors) are received by the DFE after a symbol is detected, but other reflections of a symbol (precursors) are received by the DFE before the symbol is due to be detected. A conventional DFE is unable to compensate for precursor ISI in the detection of the present symbol because of the causal nature of the feedback filter.

For example, in a sequence of ten symbols, the DFE may be working on detecting (deciding) the fifth symbol. However, precursor ISI from the sixth and seventh symbols and post-cursor

ISI of the third and fourth symbols may contribute to distortion of the fifth symbol. Since the third and fourth symbols have already been decided by the decision circuit, the feedback loop can be used to remove the postcursor ISI. However, since the sixth symbol has not been detected yet, the feedback filter does nothing to remove the precursor ISI.

There is therefore a need in the art for improved receivers and transmitters for use in communication networks. In particular, there is a need in the art for improved decision feedback equalizers that have a lower detected symbol error rate. More particularly, there is a need for receivers containing decision feedback equalizers (DFEs) that are capable of at least partially minimizing precursor ISI due to symbols that have not yet been detected. Moreover, there is a need for improved transmitters and data networks that are capable of maximizing the performance of receivers that contain decision feedback equalizers capable of reducing precursor ISI.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide an apparatus for reducing a precursor ISI signal for use in a receiver capable of receiving from a transmission channel an incoming stream of known symbols and unknown symbols distorted by intersymbol interference (ISI). In an advantageous embodiment of the present invention, the apparatus for reducing a precursor ISI signal, comprises: 1) a decision feedback equalizer capable of receiving the incoming stream of distorted known symbols and distorted unknown symbols and generating a sequence of detected symbols; and 2) a known symbol generator capable of generating a copy of a first known symbol prior to an estimation of the first known symbol by the decision feedback equalizer, wherein the decision feedback equalizer uses the copy of the first known symbol to reduce a first precursor ISI signal in a second symbol transmitted prior to the first known symbol.

According to one embodiment of the present invention, the decision feedback equalizer comprises a forward filter capable of receiving the incoming stream of distorted known symbols and distorted unknown symbols and generating an equalized output

comprising a first estimated sequence of known symbols and unknown symbols.

According to another embodiment of the present invention, the decision feedback equalizer further comprises a first feedback filter capable of receiving the sequence of detected symbols and generating a first feedback signal capable of reducing in the second symbol a first postcursor ISI signal caused by a first detected symbol transmitted prior to transmission of the second symbol.

According to still another embodiment of the present invention, the decision feedback equalizer further comprises a first summation circuit capable of summing the equalized output from the forward filter and the first feedback signal from the first feedback signal to produce a combined output.

According to yet another embodiment of the present invention, the decision feedback equalizer further comprises a symbol estimator capable of quantizing the combined output from the first summation circuit to thereby generate the sequence of detected symbols.

According to a further embodiment of the present invention, the decision feedback equalizer further comprises a second feedback filter capable of receiving the first known symbol from the known

symbol generator and generating a second feedback signal capable of reducing the first precursor ISI signal in the second symbol.

According to a still further embodiment of the present invention, the decision feedback equalizer further comprises a second summation circuit capable of summing the first feedback signal and the second feedback signal.

According to a yet another embodiment of the present invention, the transmission channel is one of a wireline channel and a wireless channel.

The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Before undertaking the DETAILED DESCRIPTION, it may be

advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior, as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

FIGURE 1A illustrates an exemplary wireline network according to one embodiment of the present invention;

FIGURE 1B illustrates an exemplary wireless network according to one embodiment of the present invention;

FIGURE 2 illustrates selected portions of exemplary transmitter circuitry disposed in the transmitting stations and, for two-way systems, the receiving stations in FIGURES 1A and 1B;

FIGURE 3 illustrates selected portions of exemplary receiver circuitry disposed in the receiving stations and, for two-way systems, the transmitting stations in FIGURES 1A and 1B;

FIGURE 4 illustrates an exemplary precursor cancellation decision feedback equalizer in a receiver according to one embodiment of the present invention; and

FIGURE 5 is a flow diagram illustrating the operation of the transmitters and receivers in the exemplary wireline and wireless networks according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURES 1 through 5, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged receiver.

Many wireline and wireless communication systems transmit a known sequence of symbols, called a training sequence, along with the unknown sequence of user data symbols in order to synchronize and adjust the receiver. The timing and values of the symbols in the training sequence are known by the receiver, thereby making the training sequence relatively easy to detect. An adaptive algorithm controller in the receiver analyzes the received training sequence, compares it to the known sequence, and uses the statistical properties of the received signal to adjust the values of the weighting coefficients in the forward filter and feedback filter of the DFE. When the unknown symbols are received, the DFE is better able to detect the correct values of the user data symbols. The present invention takes advantage of the transmission of known

symbols to provide an improved receiver that at least partially reduces precursor ISI. Furthermore, the present invention also provides an improved transmitter that transmits the known symbols in an optimum manner to take advantage of the ability of the receiver to reduce the precursor ISI.

FIGURE 1A illustrates exemplary wireline network 100 according to one embodiment of the present invention. Wireline network 100 comprises transmitting station 110 and receiving stations 121, 122 and 123. Transmitting station 110 communicates with receiving station 121-123 via wirelines 111, 112 and 113. The words "transmitting" and "receiving" with respect to transmitting station 110 and receiving stations 121-123 are exemplary only and should not be construed to limit the scope of the invention to one-way communication. In fact, in advantageous embodiments of the present invention, transmitting station 110 may comprise transceiver circuitry capable of transmitting data to, and receiving data from, receiving stations 121-123. Accordingly, in such embodiments, receiving station 121-123 also may comprise transceiver circuitry capable of transmitting data to, and receiving data from, transmitting station 110. Both transmitting station 110 and each of receiving stations 121-123 transmit data to a receiving device as mixture of known symbol sequences (e.g.,

training sequences) and unknown symbols (i.e., user data).

By way of example, in one embodiment of the present invention, transmitting station 110 may comprise a server in a local area network (LAN) or wide area network (WAN) that communicates bidirectionally with client nodes (i.e., receiving stations 121-123). In an alternate embodiment of the present invention, transmitting station 110 may comprise a cable television broadcast system that primarily transmit video signals to cable set-top boxes (i.e., receiving stations 121-123) in subscriber homes. However, transmitting station 110 may also receive upstream data traffic transmitted by the cable set-top boxes (STBs).

FIGURE 1B illustrates exemplary wireless network 150 according to one embodiment of the present invention. Wireless network 150 comprises transmitting station 160 and receiving stations 171, 172 and 173. Transmitting station 160 communicates via the air interface with receiving station 171-173. Again, the words "transmitting" and "receiving" with respect to transmitting station 160 and receiving stations 171-173 are exemplary only and should not be construed to limit the scope of the invention to one-way wireless communication. In fact, in advantageous embodiments of the present invention, transmitting station 160 may comprise transceiver circuitry capable of wirelessly transmitting data to,

and wirelessly receiving data from, receiving stations 171-173. Accordingly, in such embodiments, receiving station 171-173 also may comprise transceiver circuitry capable of wirelessly transmitting data to, and wirelessly receiving data from, transmitting station 160. Both transmitting station 160 and each of receiving stations 171-173 transmit data to a receiving device as mixture of known symbol sequences (e.g., training sequences) and unknown symbols (i.e., user data).

By way of example, in one embodiment of the present invention, transmitting station 160 may comprise a server in a wireless LAN or WAN that communicates bidirectionally with client nodes (i.e., receiving stations 171-173). In an alternate embodiment of the present invention, transmitting station 160 may comprise a base transceiver station in a cellular network that transmits voice and data traffic to mobile stations (i.e., receiving stations 171-173) and receive voice and data traffic from the mobile stations (e.g., cell phones). In still another embodiment of the present invention, transmitting station 160 may comprise a high definition television (HDTV) broadcast facility that transmits high definition video signals to HDTV receivers (i.e., receiving stations 171-173) in its local coverage area.

In both wireline network 100 and wireless network 150, each

transmitted data symbol arrives at the receiving device distorted by postcursor and precursor intersymbol interference (ISI) caused by the band-width limited transmission channel and or reflections off objects. To minimize the effects of ISI, receiving stations 121-123 and receiving stations 171-173 comprise adaptive decision feedback equalizers (DFEs) capable of reducing both postcursor ISI and precursor ISI in accordance with the principles of the present invention. Furthermore, in bidirectional communication networks, transmitting stations 110 and 160 also may comprise adaptive DFEs capable of reducing both postcursor ISI and precursor ISI in signals transmitted by receiving stations 121-123 and receiving stations 171-173.

FIGURE 2 illustrates selected portions of exemplary transmitter circuitry disposed in transmitting stations 110 and 160 and, for two-way systems, receiving stations 121-123 and 171-173. The exemplary transmitter circuitry comprises outgoing data source 205, calibration/training bits generator 210, known symbol distribution controller 215, multiplexer 220, symbol encoding circuitry 225, up-converter/modulation circuitry 230, and transmitter front-end circuitry 235. Outgoing data source 205 generates the user data that is to be transmitted to a receiving device. For example, outgoing data source 205 may be a cell phone

vocoder that converts an analog voice signal to digital data to be transmitted to a base transceiver station. Alternatively, outgoing data source 205 may be an application executed on a server that transmits data to a client work station via a wireline LAN.

The user data generated by outgoing data source 205 are unknown data bits that are combined with known data bits generated by calibration/training bits generator 210. Calibration/training bits generator 210 may generated a training sequence that precedes the unknown user data. Calibration/training bits generator 210 also may generate additional training sequences that are distributed among the unknown data as a single block or in a plurality of smaller blocks at known intervals or locations among the unknown user data. For example, in a GSM mobile phone network, a GSM data packet comprises 148 bits, including 116 user data bits. The GSM data packet also comprises 3 start bits at the start of the user data, a 26-bit training sequence in the middle of the user data bits, and 3 stop bits at the end of the user data bits.

The size and location of the training/calibration sequences of known data bits are controlled by known symbol distribution controller 215, which selectively switches the source of data that is output by multiplexer (MUX) 220. Thus, the output of MUX 220 is a stream of known calibration/training bits interspersed at known

locations among unknown user data bits. In an advantageous embodiment of the present invention, known symbol distribution controller 215 is an adaptive device that is capable of modifying the size and location of groups of calibration/training bits according to the known characteristics of the receiver. More particularly, known symbol distribution controller 215 is capable of modifying the size and location of groups of calibration/training bits in order to maximize the performance of the improved precursor ISI cancellation decision feedback equalizer (DFE) in the receiving device.

Symbol encoding circuitry 225 encodes the data bits according to any known symbol encoding scheme. Thus, a Logic 1 bit received from multiplexer 225 may be encoded as a first unique sequence of pulses and a Logic 0 bit received from multiplexer 225 may be encoded as a second unique sequence of pulses. Thus, the output of symbol encoding circuitry 225 is the sequence of known and unknown symbols that must be detected by the receiver DFE.

Up-converter/modulation circuitry 230 converts the baseband sequence of known and unknown symbols to a modulated (up-converted) signal capable of being transmitted through the transmission channel (wireline or wireless). For example, in a wireless network, up-converter/modulation circuitry 230 may comprise an RF

mixer that converts the baseband sequence to a modulated radio frequency (RF) signal capable of being transmitted through the air channel to a receiving device. Finally, transmitter front-end circuitry comprises RF amplifiers, duplexer circuitry, and antennas that transmit the output of up-converter/ modulation circuitry 230 into the corresponding wireline or wireless channel.

The arrangement and interconnection of known symbol distribution controller 215, calibration/training bits generator 210, and symbol encoding circuitry 225 is exemplary only. Those skilled in the art will recognize there are numerous other circuit arrangements capable of inserting known symbols at known locations in a sequence of outgoing unknown symbols. The arrangement in FIGURE 2 is suitable for those applications in which a symbol is used to represent no more than one data bit. This ensures that a known bit from calibration/training bits generator 210 is encoded only as a known symbol and that an unknown bit from outgoing data source 205 is encoded only as an unknown symbol.

However, in other systems, a single symbol may be used to represent more than one data bit. For example, four different symbols may be used to represent the bit pairs 00, 01, 10, 11. In such a system, precautions must be taken to ensure that symbol

encoding circuitry 225 does not encode a known bit and an unknown data bit as a single symbol. To accomplish this, known symbol distribution controller 215 and calibration/training bits generator 210 may be coupled directly to symbol encoding circuitry 225, and multiplexer 220 may be omitted. In such a circuit arrangement, symbol encoding circuitry 225 would encode all unknown data bit pairs from outgoing data source 205 as a sequence of unknown symbols and known symbol distribution controller 215 would cause symbol encoding circuitry 225 to insert known symbols representing known data bit pairs into the outgoing sequence of unknown symbols.

FIGURE 3 illustrates selected portions of exemplary receiver circuitry disposed in receiving stations 121-123 and 171-173 and, for two-way systems, transmitting stations 110 and 160. The exemplary receiver circuitry comprises receiver front-end (F-E) circuitry 305, down-converter/demodulation circuitry 310, bandpass (BP) filter 315, sampler circuitry 320, precursor decision feedback equalizer (PC-DFE) 325, timing synchronization circuitry 330, adaptive algorithm controller 335, and receiver processing circuitry 340. Receiver front-end circuitry 305 typically comprises a low noise amplifier and filters that receive the transmitted known and unknown symbols from the wireline or wireless

channels and amplify and isolate the frequencies of interest (i.e., receive band).

Down-converter/demodulation circuitry 310 demodulates (down-converts) the incoming modulated signals to produce an analog baseband signal comprising a sequence of known and unknown symbols that are distorted to postcursor and precursor ISI. Sampler circuitry 320 converts the analog baseband signal to a digital baseband signal. The digital baseband signal is filtered by PC-DFE 325 to minimize the postcursor and precursor ISI distortion. Ideally, the output of PC-DFE 325 is the original sequence of known and unknown symbols.

Timing synchronization circuit 330 receives the output of PC-DFE 325 and uses it to synchronize (align) the analog-to-digital converter in sampler circuitry 320 and to synchronize the filtering circuitry in PC-DFE 325, as described below in greater detail. Adaptive algorithm controller 335 also receives the output of PC-DFE 325 and compares it to the input sequence of distorted symbols from sampler circuitry 320. From this comparison, adaptive algorithm controller 335 can determine and modify the weighting coefficients in the forward filter section and the feedback filter section of PC-DFE 325 in order to minimize ISI distortion. Finally, receiver processing circuitry 340 converts the sequence of known

(i.e., calibrations/training) symbols and unknown symbols back to data bits and extracts the user data bits according to the algorithm used by known symbol distribution controller 215.

FIGURE 4 illustrates exemplary precursor cancellation decision feedback filter (PC-DFE) 325 in greater detail according to one embodiment of the present invention. PC-DFE 325 comprises forward filter 405, summer 410, symbol estimator 415, feedback filter 420, summer 425, feedback filter 435 and known symbol generator 430 according to one embodiment of the present invention. Those skilled in the art will recognize that forward filter 405, summer 410, symbol estimator 415, and feedback filter 420 constitute a conventional decision feedback filter capable of reducing postcursor ISI from previously estimated (or decided) symbols. The present invention differs from a conventional decision feedback filter due to the addition of summer 425, feedback filter 435, and known symbol generator 430.

As noted above, adaptive algorithm controller 335 determines the values of the weighting coefficients, Ci, of forward filter 405, the weighting coefficients, Cm, of feedback filter 420, and the weighting coefficients, Cn, of feedback filter 435. Adaptive algorithm controller 335 estimates the channel impulse response during receipt of the known training symbols and during

receipt of other known symbols, such as known synchronization symbols and known packet identification symbols. If a training sequence is used, forward filter 405, feedback filter 420 and feedback filter 435 may be adaptively adjusted using the recursive least square (RLS) algorithm or the least mean square (LMS) algorithm.

Forward filter 405 receives the sequence of ISI-distorted symbols, Y_k, from sampler circuit 320 and produces an equalized output, Y'_k, that is an estimate of the input sequence. Adder 410 add the Y'_k output to a composite (precursor and postcursor) ISI correction signal (explained below in greater detail) from summer 425 to produce the symbol estimate, v_k. Symbol estimator 415 quantizes the v_k symbol estimate to the nearest symbol value to form a sequence of decided (i.e., detected) symbols, $\hat{S}_{k-d}$, that is transmitted to timing synchronization circuitry 330, adaptive algorithm controller 335, and receiver processing circuitry 340. The quantity k is the index of the current symbol and d is the decision (detection) delay associated with symbol estimator 415. The decided symbol sequence also is transmitted back to feedback filter 420, which removes that part of the intersymbol interference from the present estimate caused by previously detected symbols (i.e., post-cursor ISI).

Known symbol generator 430 receives a timing signal from timing synchronization circuitry 330 and transmits a sequence of known symbols, S'_k, through feedback filter 435 at the proper location in the sequence of known and unknown symbols that are being processed by symbol estimator 415. In an advantageous embodiment of the present invention, feedback filter 435 is a L_2-tap transversal filter chosen to minimize precursor ISI from the known symbols. The output of known symbol generator 430 is normally zero. However, known symbol generator 430 generates known symbols during the time periods when one or more preceding unknown symbols are being estimated by symbol estimator 415. In this manner, the effect of the precursor ISI of the known symbol can be removed from the present estimate, even though the known symbol has not been detected yet.

For example, if the sixth symbol in a sequence is known, known symbol generator 430 can output the sixth symbol during the estimation of the unknown fourth symbol and the unknown fifth symbol. The precursor ISI of the sixth symbol can therefore be removed from, for example, the fifth symbol estimate, just as feedback filter 420 removes from the fifth symbol estimate the postcursor ISI of the fourth symbol.

FIGURE 5 depicts flow diagram 500, which illustrates the

operation of exemplary transmitting stations 110 and 150 and exemplary receiving stations 121-123 and 171-173 in wireline network 100 and wireless network 150 according to one embodiment of the present invention. Transmission of user data begins when, for example, transmitting station 110 transmits a training sequence of known symbols to receiving station 121 (process step 505). Next, adaptive algorithm controller 335 in receiving station 121 adjusts the coefficients of the filters in PC-DFE 325 to achieve, for example, minimum mean square error (process step 510). By the end of the training sequence, PC-DFE 325 uses the output of symbol estimator 415 in feedback filter 420 to minimize postcursor ISI in subsequent unknown user data symbols (process step 515). At the same time, PC-DFE 325 uses the output of known symbol generator 430 in feedback filter 435 to minimize precursor ISI in subsequent unknown user data symbols (process step 520).

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.